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Development of an ear-level digital hearing aid and computer-assisted fitting procedure: An interim report*

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Abstract—Recent progress on the development of an ear-level digital hearing aid is described. The work includes development of a body-wearable digital hearing aid and a computer-based hearing evaluation system that exploits the flexibility afforded by digital signal processing. The prescriptive criteria and fitting procedure used with the digital hearing aid are described briefly. Design considerations in the development of VLSI chips for an ear-level unit are discussed.

INTRODUCTION

Hearing assessment and hearing aid selection is complicated and is prone to errors of measurement and calibration. The problem is twofold. First, commercial hearing aids do not have the amount of adjustment flexibility, with regard to frequency-dependent maximum power output and gain, that is required to fit certain patients. Second, traditional fitting methods in which the hearing aid and audiometer are calibrated in separate test fixtures, independently of the patient, can introduce significant errors of measurement (4).

The use of a programmable hearing aid in conjunction with a computer-assisted fitting procedure can eliminate these fundamental problems, and therefore has the potential for significantly improving hearing aid performance for a large number of patients. The use of a hearing aid that can be programmed to operate over a wide range of frequency-dependent gain and maximum power output functions will permit better utilization of the patient's residual hearing. The use of automatic testing procedures to determine the patient's hearing threshold, uncomfortable loudness level, and most comfortable loudness level—while the patient is wearing the aid—eliminates common sources of measurement error and enables the audiologist to establish a desired hearing aid prescription quickly and more precisely.

Digital signal processing methods offer great potential for adjustment flexibility and precision of fit. With relatively simple digital processing structures, it is possible to provide a wide range of filter configurations that can be programmed to optimize the performance of the aid with regard to the patients' hearing impairment. Furthermore, digital technology opens the door for the designer to use more sophisticated processing algorithms such as adaptive feedback equalization and noise reduction.

The hearing aid model that is under development is a multichannel, instantaneous compression aid based on the work of Miller et al. (4), Skinner (9), Skinner et al. (10), and Pascoe (7). In this model,

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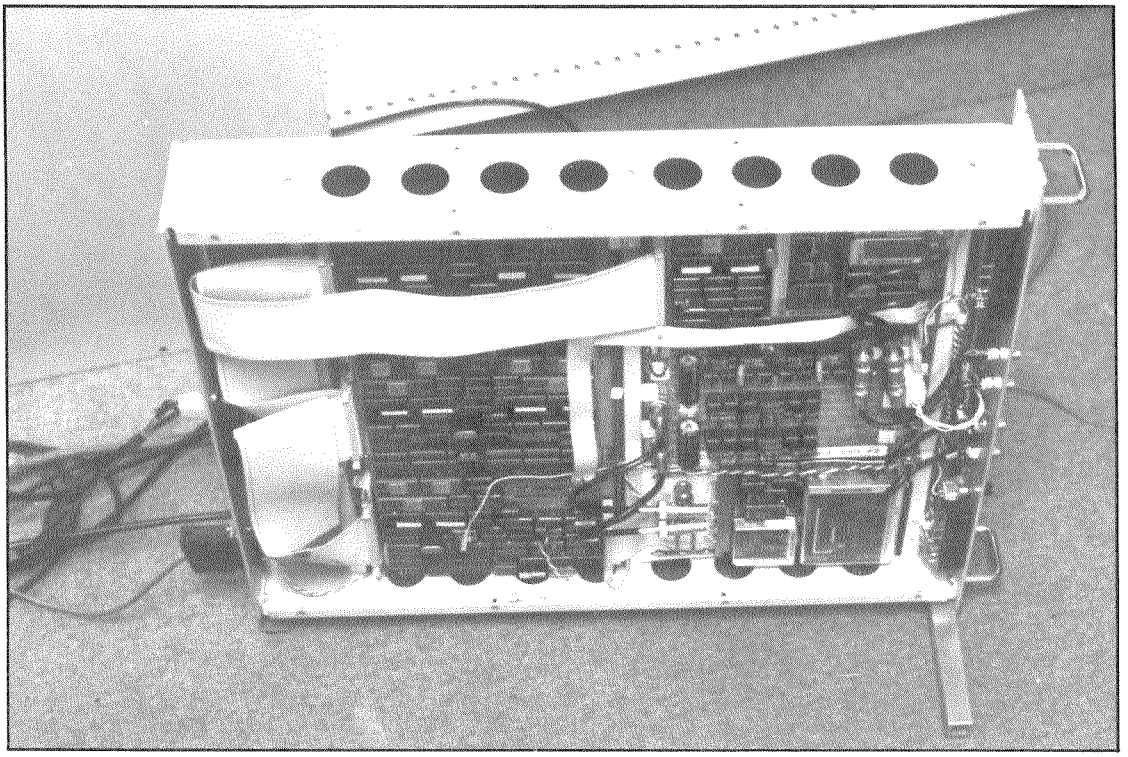

Figure 1.
Laboratory-based digital hearing aid system. System contains six TMS320 microprocessors and can execute 15 million multiply-accumulate operations per second. Application programs are downloaded from a host computer and operate in real time.

the signal spectrum is divided into four contiguous bands of frequencies. Within each band, the gain and maximum power output can be adjusted independently. Distortion caused by the instantaneous compression is minimized by a second stage of bandpass filters. In fitting the aid, the gain parameters are chosen to provide spectral shaping and balance appropriate for the patient. The compression parameters are chosen to provide an appropriate frequency-dependent maximum power output characteristic. Overall gain control is also provided to prevent excessive compression action at high signal levels.

This hearing aid model has been implemented on both a laboratory-based digital system and a wearable digital system. Both systems utilize conventional digital processing circuitry and are of our own design. Both systems are used in conjunction with special computer-based audiometer systems, also of our own design, for testing patients and setting the parameters of the hearing aid model. Both systems can be programmed in a general way to implement various hearing aid models.

LONG-TERM GOAL

The ultimate goal of this work is to develop a new hearing aid concept that will provide significantly increased benefits to the hearing impaired. The scope of the research includes development of signal processing algorithms that are appropriate for ear-level implementation, reduction of the algorithms to VLSI circuits, development of improved fitting strategies, and clinical verification of the overall concept. A systematic approach that addresses both the engineering aspects of algorithm and chip design and the psychoacoustic aspects of hearing aid fitting can lead to rapid commercialization of the concept resulting in availability of the final device to the hearing-impaired population.

INTERIM ACHIEVEMENTS

Laboratory-based system

The laboratory-based digital hearing aid system (5, 12) shown in **Figures 1 and 2** was constructed

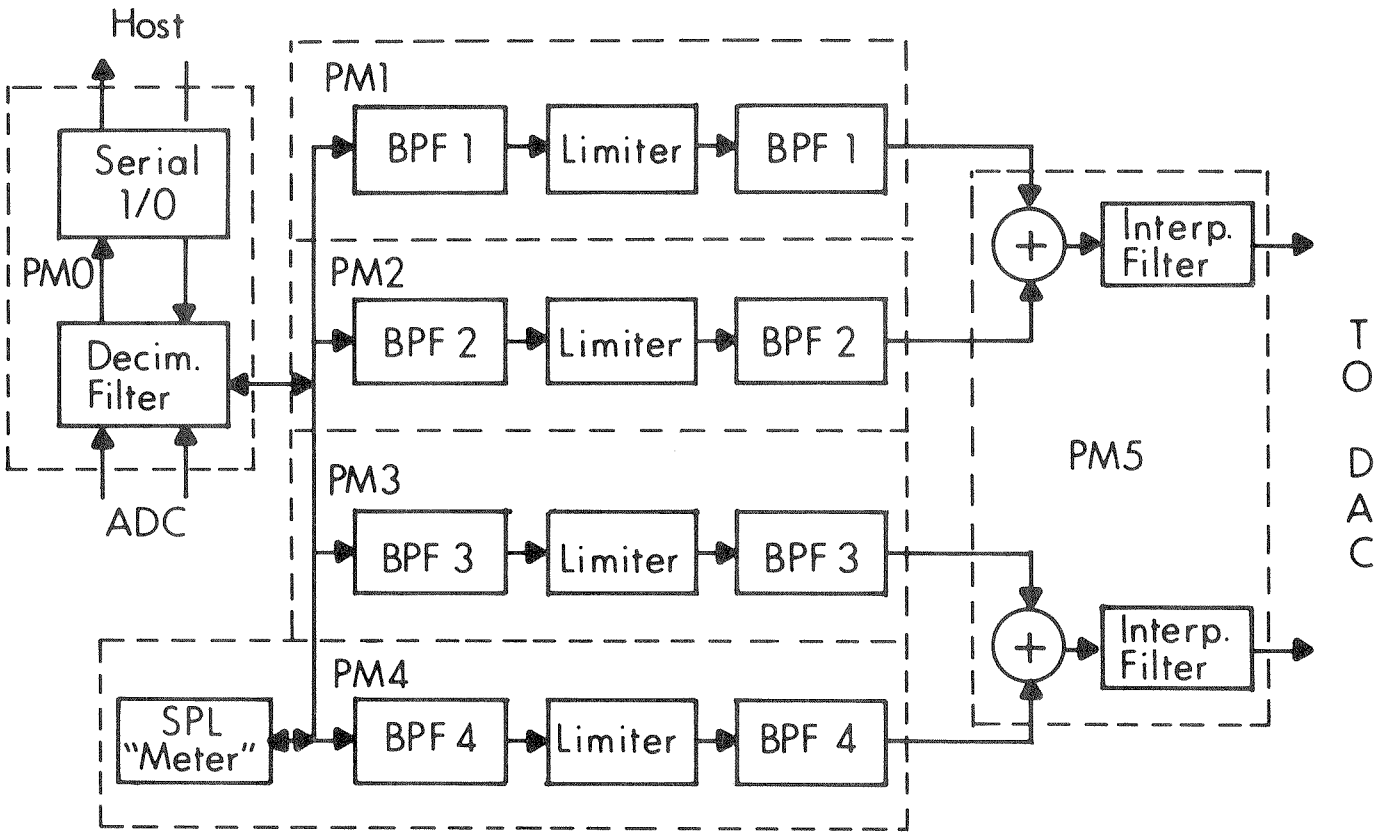

Figure 2.
Block diagram of system organization showing input processor, four general processors, and output processor. System has two input and two output channels. All channels can be operated simultaneously at 50 kilohertz sampling rates and have a signal-to-noise ratio and dynamic range of greater than 80 dB.

from conventional parts and includes two input channels (one for the signal microphone and one for the probe microphone), two output channels (one for the low-frequency receiver and one for the high-frequency receiver), and a serial communication interface that connects to the computer-based audiometer. It contains six conventional integrated circuits (TMS320 digital signal processors) which can be programmed from the host computer in the audiometer system to implement a variety of signal processing algorithms. High performance real-time operation has been emphasized in the design of this system so that the simulation of the hearing aid is not limited in any practical sense by processing noise or dynamic range.

The analog-to-digital and digital-to-analog converters of the system are 16-bit linear pulse code modulation (PCM) converters with a dynamic range of 96 dB. The harmonic distortion is less than .005 percent. Each of the two input and output channels can be sampled at a maximum of 50,000 samples per second. The resulting signal bandwidth for each channel can therefore be as wide as 25,000 Hz. The total computational capacity of the system is 15 million multiply-add operations per second, making it possible to implement a wide variety of practical digital filter designs in real time.

A program that has been written for the system to implement the four-channel, instantaneous compression hearing aid model provides for independent settings of gain and maximum power output for each channel. The program communicates with the host computer of the audiometer system so that the gain and maximum power output of each channel can be independently programmed by the host computer to fit a particular hearing impairment. In addition, a second version of the program has been developed that varies the dynamic range of the model in order to make perceptual determinations of its significance.

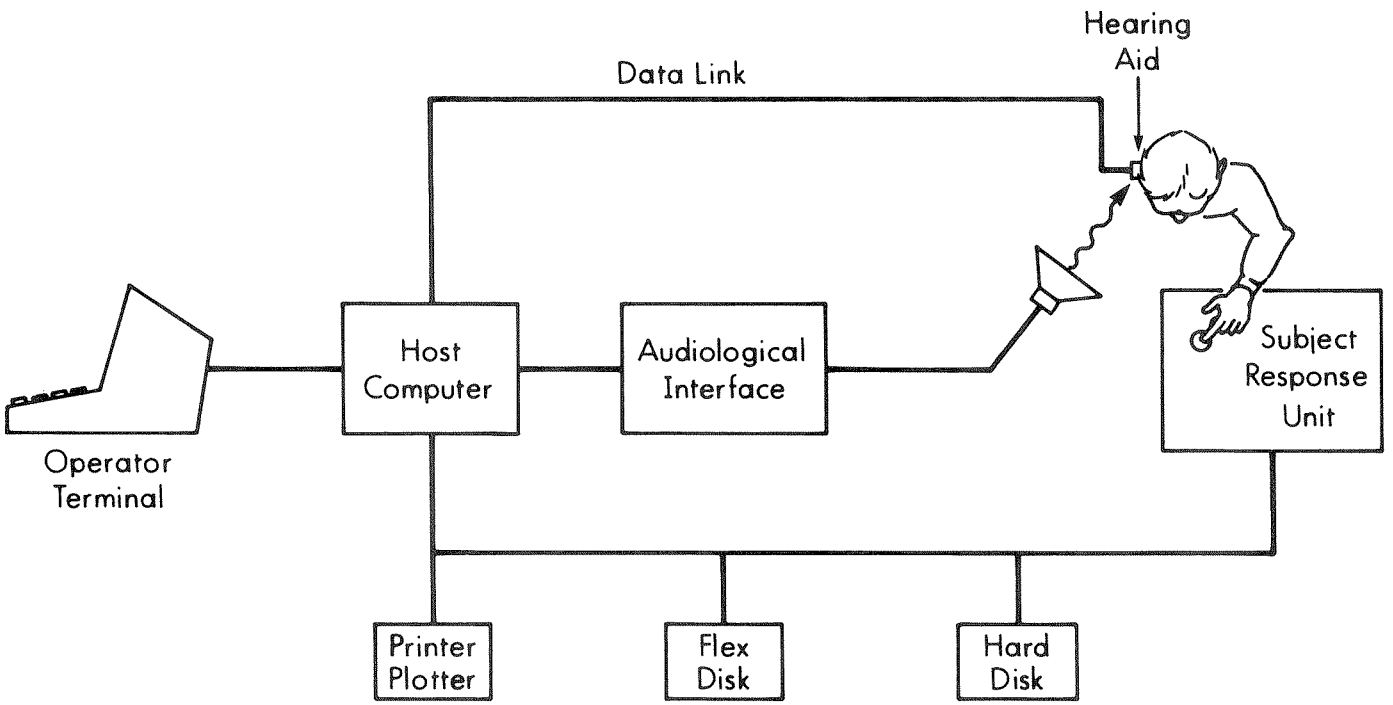

Figure 3.
Schematic diagram of computer-based audiometer system. With this system, stimulus sounds are played in any desired sequence to the subjects. The sound level of the presentation is controlled by programmable attenuators located in the audiological interface. The subjects respond via the touch-screen terminal and their responses are automatically recorded and analyzed. The characteristics of the hearing aid are controlled automatically.

Computer-based audiometer system

A computer-based audiometer system shown in **Figure 3** was developed to use in conjunction with the digital hearing aid system. It uses a PDP-11 computer with 10 Mbytes of hard disk storage, analog-to-digital and digital-to-analog interfaces, operator terminal with graphics capability, printer for both text and graphics, a touch-screen subject terminal, an audiological interface for controlling signals in audiological testing, and a serial communication port for control of the digital hearing aid. With this system, sounds are stored on the hard disk and can be played in any desired sequence to the subjects. The sound level of the presentation is controlled by programmable attenuators located in the audiological interface. The subjects respond via the touch-screen terminal and their responses are automatically recorded and analyzed and the characteristics of the hearing aid are controlled automatically.

Programs for the system have been completed for measuring threshold and uncomfortable loudness levels as functions of frequency. The test sequence is controlled by the host computer as a function of the patient's responses. In addition, the following programs have been written: 1) a program for recording, editing, and creating disk files of sounds; 2) a program that implements the MEGS* speech test (3) that was developed at the Central Institute for the Deaf (CID) for testing subject's ability to discriminate all phonetic sounds of general American English; 3) a program for testing subjects using the CUNY Nonsense Syllable Test (8); 4) a program for measuring and graphically displaying the patient's auditory area along with the hearing aid prescription; and 5) a main program and a library of Fortran subroutines that control and communicate with the digital hearing aid. These programs are accessed from a menu-driven display that is self-explanatory and provides help information for the inexperienced operator.

*The name of the test, MEGS, was derived from the names of the developers.

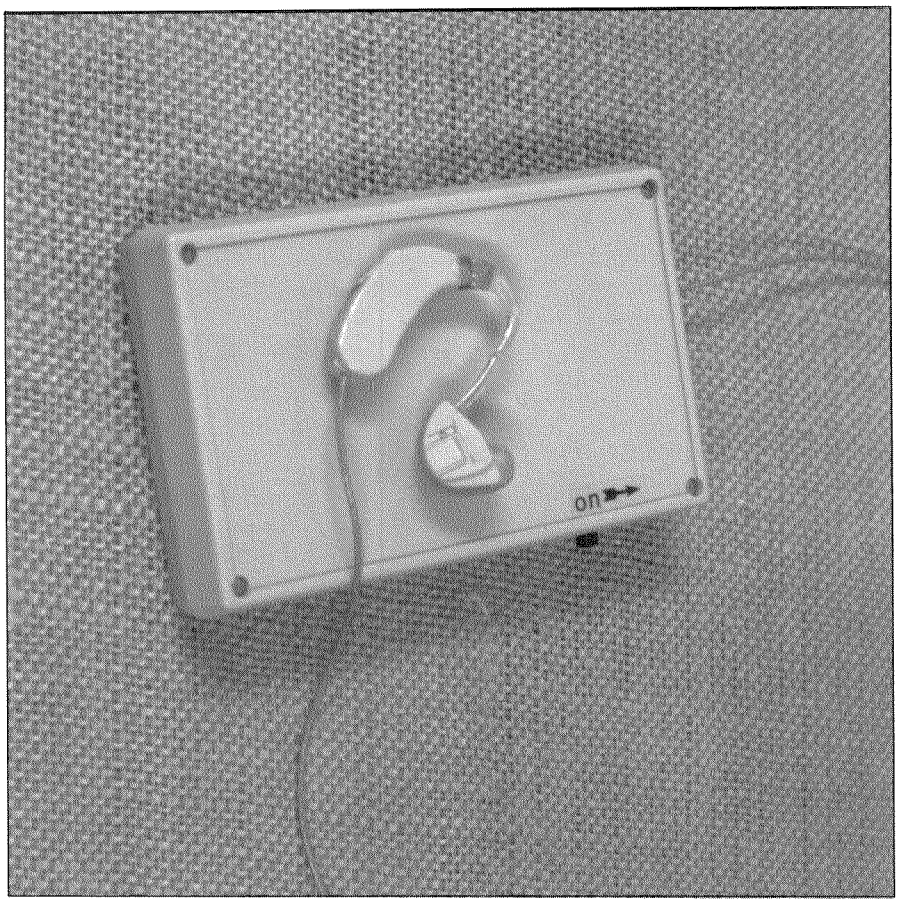

Figure 4.
Wearable digital hearing aid. The aid can be programmed to model a variety of hearing aid models.

Wearable digital hearing aid system

In order to test the digital hearing aid concept further under more natural conditions of signal and noise, a wearable version of the digital hearing aid has been developed from commercially-available components (2). This system, which is shown in **Figure 4**, has been programmed to implement the four-channel instantaneous compression model. The program also includes routines for stimulus generation and sound measurement. During the fitting procedure the wearable digital hearing aid is connected to a host computer via a serial port to control the presentation of stimulus sounds within the aid, to monitor the sound pressure in the patients' ear through the probe channel of the hearing aid, and to adjust the parameters of the aid. Like the laboratory-based system, the wearable system includes a probe microphone to measure sound pressure in the patient's ear. These sound pressure measurements are available to the host computer during the test. The host is also connected to a conventional digitally-controllable audiometer.

The wearable system is a general-purpose digital signal processing system. It consists of a digital signal processor circuit board, analog electronic circuit board, and a battery with a capacity of about 10 hours, all fitting into a case which is 5.5 inches long, 3.5 inches wide, and 1.2 inches thick. The processor circuit board contains a digital signal processor (Fujitsu MB8764), random access memory (RAM) for program instructions and data, and circuitry for switching from main power to standby power when the main power source is interrupted. The MB8764 is well-suited for processing audio signals. It has a single-cycle, pipelined, 16 by 16 bit multiply-add instruction that is effective in implementing digital filters, and a 16-bit parallel data bus for connection to external devices. Program and data can reside in external memory for development purposes.

The processor circuit board includes the serial data port that can be connected to a host computer during patient testing. The final hearing-aid parameters are downloaded from the host to the wearable

Figure 5.
Ear module. The behind-the-ear unit contains preamplifiers for the signal and probe microphone. The in-the-ear unit contains signal and probe microphones and receiver.

hearing aid through this port.

The hearing aid circuit board includes a signal channel with a preamplifier with programmable gain and a probe channel which is simpler, and consists of a fixed-gain preamplifier only. Both channels share a two-channel, track-and-hold multiplexer and an eight-bit analog-to-digital converter of a Codec chip. Through companding,* the Codec chip provides a 70 dB input dynamic range at sufficiently high sample rates and low power. A conversion table is included in the MB8764 program to convert the mu-law compressed input data into linear form for processing. The hearing aid output channel utilizes the digital-to-analog converter of the Codec chip and includes a programmable-gain power amplifier for driving the hearing aid receiver in the ear module.

The body unit is connected, via a flexible cable, to an ear module that resembles an ear-level hearing aid and that contains the various transducers and preamplifier circuitry (See **Figure 5**). The hearing aid circuitry includes analog signal conditioning, programmable input and output range selection, and analog-to-digital and digital-to-analog converters.

External connections from a host computer system to the processor board provide for direct access to the three program RAMs during the program downloading operation. This is a one-time process and the external cables are replaced with jumper connectors that connect the instruction and address bus of the RAMs to the MB8764 in normal use. This design approach was implemented in order to minimize the logic required to switch the RAMs between

*Companding refers to the process of compressing the signal amplitude before conversion from analog to digital form and expansion of signal amplitude after conversion from digital to analog form in order to achieve a more efficient digital representation.

the off-board host computer and the MB8764.

A cross assembler has been written for a PDP-11 host computer system so that application software can be developed on the host and downloaded to the program RAMs of the wearable digital hearing aid as described above. Program integrity is maintained, thereafter, by a small battery that is permanently installed on the processor board and that provides standby power in the event that the primary power source becomes discharged or is removed. The power consumed by the processor board, including microprocessor and memories, when operated at a 5 megahertz rate, is 225 milliwatts. Standby current required to preserve the contents of the program and data memories is about 40 microamperes. The standby battery, which has a capacity of 40 milliampere-hours, therefore provides memory backup for a minimum duration of 1000 hours in the standby state. The primary battery, which provides power for both the digital and analog circuitry, is a P500 Lithium battery. It has a flat shape that is 3.7 inches long, 3.0 inches wide, and .18 inches thick and can supply 100 milliamperes of current for a continuous period of 10 hours.

The wearable hearing aid program that has been written to model the four-channel instantaneous compression model consists of eight finite impulse response filters arranged in four channels. Each channel comprises a bandpass filter, limiter, and bandpass filter. As described above, this model allows for the maximum output and gain to be separately controlled within each of the four channels to match the patient's discomfort threshold and hearing threshold, respectively. The filters reduce products of distortion that are generated by the limiting process, so that they are generally below the masked threshold of the ear within each channel.

The channels are nominally allocated frequencies of 0 to 500 hertz, 500 to 1500 hertz, 1500 to 3000 hertz and 3000 to 6000 hertz. However, the filter bandwidths and center frequencies can be adjusted while the patient is undergoing testing. The filters are implemented directly as 32-tap, finite-impulse-response filters with linear phase. The MB8764 requires 37 instructions or 7.4 microseconds to compute each of the eight filters, resulting in a total of about 60 microseconds per input sample. The time required to compute the limiting is about 2 microseconds per channel or 8 microseconds for all four channels. Other instructions (for computing sound pressure, for controlling the Codec and the serial communication shift register, and for conversion between mu-law and linear and back to mu-law data representation) require less than the remaining 12 microseconds between samples at the 12.5 kilohertz sampling rate.

The filter coefficients for all 8 filters are stored in 64 locations of internal ARAM of the MB8764. This small amount of storage is possible because the two filters in each channel are identical and the filters are symmetrical. Coefficients that determine gain and maximum output for each channel are also stored in the ARAM. Input data samples and intermediate filtered samples are stored in 160 locations of external data RAM.

The MB8764 is somewhat limited with regard to internal data memory (256) and program memory (1024). However, it is possible to model most circuits found in hearing aids and other interesting prosthetic devices by careful use of these resources. For example, at an instruction rate of 5 megahertz and a sampling rate of 12.5 kilohertz, it is possible to execute 400 instructions per sample.

Although the wearable digital hearing aid is not suitable for commercialization because of its power consumption and size, it has the potential for improving our understanding of issues of signal processing with regard to hearing aids, and, although it is possible to simulate "natural" conditions of signal and noise in the laboratory, important additional insight can be gained by wearing such a device in natural surroundings.

Very Large Scale Integrated circuit (VLSI) design

Since the ultimate goal of this research is to develop an ear-level version of the digital hearing aid, a preliminary study of VLSI digital processing designs was undertaken. An appropriate design must be small enough to fit into an ear-level package, must operate from a hearing aid battery, and must provide sufficient computational capacity to implement suitable processing algorithms.

Complementary metal oxide semiconductor (CMOS) technology is ideal for low-power hearing aid designs. CMOS circuitry can be operated from a 1.2-volt battery (11). Since the power consumption of CMOS circuitry is a function of the square of the supply voltage, circuits operated at 1.2 volts consume signifiantly less power than when operated at

the more conventional 5-volt level. The CMOS fabrication process can easily be adjusted to produce logical switching thresholds compatible with the lower 1.2 volt supply (11). Since power consumption is proportional to the active chip area, the smallest possible feature size should be used in the chip design. At this time 1.0 micron feature size CMOS circuitry can be fabricated by the semiconductor industry.

Since the power consumption of CMOS circuitry is directly related to the computational complexity of the processing algorithm, additional power savings can be achieved by optimizing the structure and the algorithm with respect to power consumption. For example, the use of a systolic processing array and a logarithmic representation of the sampled data results in a considerable saving in power. Systolic arrays* are highly concurrent processing structures that consume power only when the bit patterns within the array change. Logarithmic encoding provides a maximum dynamic range with respect to the number of bits required to represent the signal. Baker et al., (1), have analyzed the design of a 9-bit logarithmic multiplier-accumulator (LMA) cell and have shown that when fabricated in 3 micrometer CMOS technology and operated from a power supply of 5 volts, the cell would require 50 mirowatts of power and would require an active chip area of about one square millimeter. Roughly 100 LMA cells, arranged in a systolic array, can be fitted on a 10 millimeter square chip whose power consumption would be about 5 milliwatts. Such a chip can perform all of the processing required for one of the four channels in the digital hearing aid.

The design described in (1) has been refined further by Natarajan and Engel (6). They designed a single LMA cell with 8-bit architecture that is currently being fabricated in 3-micron CMOS (see **Figure 6**). It will be tested in the near future. Natarajan and Engel have estimated that the power consumption of this design will be about 20 microwatts when it is operated at 5 volts. The cell requires about 1500 transistors and occupies less than 2 square millimeters of active chip area.

This LMA cell serves as a basic computational unit for implementing one tap (multiply-add operation) of a finite impulse response (FIR) filter. Assuming that the cells are arranged in a systolic FIR filter array, it is possible to estimate the power consumption of the digital processing section of the four-channel compression aid when operating at a 12.5 kHz sampling rate and utilizing eight 32-tap filters. The total tap count is 256 and, therefore, assuming that this chip is fabricated with a 1-micron feature size and operated from a 1.5-volt battery, it would contain all 256 LMA cells in an area of approximately 49 square millimeters (7 mm sides) and consume less than 250 microwatts of power (6).

PRESCRIPTIVE CRITERIA AND FITTING PROCEDURE

The fitting procedure for the multichannel compression aid attempts to adjust the gain and maximum power output of the aid so that conversational speech falls within the most comfortable listening range for the patient and so that loud sounds are limited to fall below the discomfort level of the patient. That this achieves an optimum fit with regard to speech intelligibility and comfort is based on the research findings of Pascoe (7) and Skinner et al. (10).

The computer-based fitting procedure requires two steps that involve the patient. First, the patient's unaided hearing threshold level as a function of frequency is measured and an earmold impression taken. Second, the patient's hearing threshold level, most comfortable listening level, and uncomfortable listening level are measured through the aid and earmold. The appropriate hearing aid characteristic is determined automatically by the computer which calculates the gain and compression parameters required to maintain conversational speech within the patients' residual auditory area as bounded by the hearing threshold level and uncomfortable listening level.

An important feature of the method is that the aid is included in testing the patient. Therefore, the test results include the effects of the head, pinna, earcanal, earmold, and other factors associated with the hearing aid and the patient. For threshold measurement, the gain in the aid remains at 0 dB and calibrated stimuli presented by the loudspeaker of the audiometer are varied to determine threshold levels. For uncomfortable listening level measurements, the level of the signal to the loudspeaker is varied up to its maximum undistorted limit (around 90 dB SPL). If higher signal levels are required, the signal from the loudspeaker can be held constant

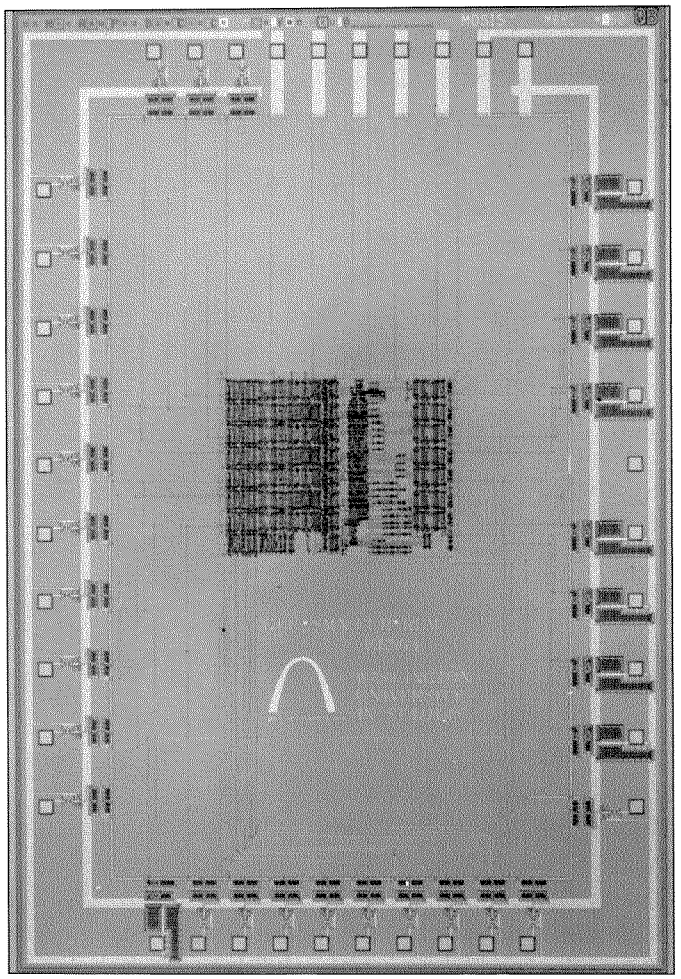

Figure 6.
Micrograph of logarithmic multiplier accumulator cell. The cell includes a PLA lookup table, coefficient registers, and various combinatorial logic circuitry.

and the gain of the aid can be increased appropriately. This arrangement allows high-intensity stimuli to be presented to the patient while employing a loudspeaker. In this way, uncomfortable listening levels can be measured accurately in a free-field sound environment while the aid is worn by the patient. From the calibration data of the digital hearing aid and the patient's test results, the desired characteristics of the aid can be computed and used to program the characteristics of the digital hearing aid.

By incorporating the self-test and sound probe features of the wearable digital hearing aid, the fitting procedure described above can be simplified further. First the probe channel, signal channel, and receiver are calibrated in a test fixture. This procedure is easily automated with a host computer connected to the aid. The calibration parameters can be stored in the aid's memory and accessed at a later time. Next, the patient is fitted with the aid using a temporary ear mold. (It is presumed that an ear impression would be taken and a permanent earmold ordered at this time.) The aid is then used in the self-test mode to measure the patient's hearing threshold. This provides a transfer function of the receiver, earmold, and patient's ear. The probe channel of the hearing aid serves as an absolute measure of the patient's threshold in terms of sound pressure level.

Next, the patient's hearing threshold, uncomfortable loudness level, and most comfortable loudness level are determined through the aid using the test stimuli generated by an audiometer. Finally, the parameters of the aid, gain and maximum power output, are adjusted.

Studies to evaluate the potential of the self-test concept and to evaluate the performance of the four-channel instantaneous compression model under natural condition of signal and noise are under way, and the results will be reported in a future paper.

SUMMARY

One approach to the development of a better hearing aid has been described. This research addresses fundamental problems of hearing aid fitting and hearing aid utilization. By developing a flexibly programmable hearing aid that is worn by the patient during the fitting procedure, errors of measurement and calibration are eliminated and more precise adjustment of the hearing aid characteristics to match the patient's auditory area is achieved.

The use of real-time processing systems to evaluate hearing aid models in the laboratory and in field studies has been discussed. The availability of real-time systems provides invaluable insights that help guide the designer in development of processing algorithms and VLSI structures.

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*Systolic arrays are arrays of processing elements in which the inputs and outputs of each element are connected only to neighboring elements to form a regular lattice structure. The term "systolic array" has become common usage and reflects the similarity between the way data propogate through the array and the systolic action of the heart and vascular system.

Lastly, the issue of size and power consumption with regard to digital signal processing has been addressed in the context of the four-channel hearing aid model. It is shown that by choosing an appropriate number representation and an appropriate VLSI technology, and by utilizing a static processing structure, it is possible to achieve a state-of-the art digital processing circuit that is appropriate for ear-level hearing aids.

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